Claim Amendments:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently Amended) The method of ~~claim 1~~claim 7 wherein:
the first data lane enable facilitates accessing a byte of data associated with the first memory address when in the first mode of operation; and
the second memory address accesses a byte wide memory.

3. (Canceled)

4. (Canceled)

5. (Currently Amended) The method of ~~claim 1~~claim 7 wherein:
the first output is the first output of a first device; and
the first and second modes of operation utilize the first output to access a second device external the first device.

6. (Previously Presented) The method of claim 5 further comprising:
when in a third mode of operation, utilizing the first output to provide information about a memory access internal to the device that includes the first output.

7. (Previously Presented) A method comprising:
when in a first mode of operation, utilizing a first output to provide a first data lane enable for facilitating access of a portion of a first memory storage location associated with a first memory address; and
when in a second mode of operation, utilizing the first output to provide an address bit of a second memory address for facilitating designation of a second memory storage location, wherein the address bit is an additional address bit used to extend an

address range when a memory having a width less than a word width is being accessed.

8. (Currently Amended) The method of ~~claim 1~~claim 7, further comprising:

determining a mode of operation to be one of the first mode of operation and the second mode of operation.

9. (Previously Presented) The method of claim 8, wherein:

determining the mode of operation is based upon a register value associated with a specific chip select.

10. (Currently Amended) The method of ~~claim 1~~claim 7 further comprising:

when in the first mode of operation, utilizing a second output to provide an address bit of the first memory address for facilitating designation of the first memory storage location; and

when in the second mode of operation, utilizing the second output to provide a second data lane enable for facilitating access of a portion of the second memory storage location associated with the second memory address.

11. (Previously Presented) A method of providing data to a set of pins of a device, the set of pins coupled to a memory, the method comprising:

during a first mode of operation, multiplexing a first set of data onto the set of pins to allow the set of pins to provide data representing two least significant bits of a first address, a most significant bit of the first address, and a lane enable;

during a second mode of operation, multiplexing a second set of data onto the set of pins to allow the set of pins to provide data representing one least significant bit of a second address, a most significant bit of the second address, and two lane enables; and

during a third mode of operation, multiplexing a third set of data onto the set of pins to allow the set of pins to provide four lane enables.

12. (Original) The method of claim 11, wherein the first, second and third sets of data facilitate an external memory access, wherein the external memory access is external relative to the device.

13. (Previously Presented) The method of claim 12, further comprising:
during a fourth mode of operation multiplexing a fourth set of data onto the set of pins to allow the set of pins to provide information relating to an internal memory access.

14. (Previously Presented) The method of claim 11 further comprising:
determining the mode of operation is based upon a chip select indicator.

15. (Previously Presented) An apparatus comprising:
a set of address nodes coupled to a memory to provide address data for address bit locations A(n) through A(2), where A(n) represents a most significant bit for at least a first mode of operation;
a first output node coupled to the memory to provide one of an address data for address bit location A(1) and a data lane enable signal based upon a mode of operation;
a second output node coupled to the memory to provide one of an address data for address bit location A(0) and a data lane enable signal based upon the mode of operation; and
a third output node coupled to the memory to provide one of an address data for address bit location A(n+1) and a data lane enable signal based upon the mode of operation.

16. – 21. (Canceled)